# Data Requirements for CheckSum Fixture Quoting and Development

## The more data you can provide, the more accurate your quote will be

The main cost factors for test fixtures are the number of probes (= nets) and the number of components (if CheckSum is supplying the test program). The test fixture and program cost can be estimated (budgetary quote) from either a BOM or a Schematic (2 pages or less).

CheckSum will quote your project from just the above data in a budgetary "worst case" estimate, assuming probes on both top and bottom, and assuming probes of all sizes (50, 75, 100-mil).

See Page 2 for a list ofthe optimum CAD files which will provide you with testability analysis at time of quote. If you have specific requests, please list them in the e-mail requesting the quote. The following is a list of items that need to be considered for fixture quoting:

- Fixture kit (Press) type
- Quantity of boards in panel
- Quantity of separate boards using same fixture
- Additional test program versions
- ESD materials (adds around $1K to project)
- TestJet
- Fixture Counter
- Barcode scanner installation in fixture
- Marker probes
- Switch probes or differential probes for part presence verification
- Board presence sensor
- Switch activation (spring-loaded)
- Switch activation (automated)
- Power tests (please specify)
- Functional tests (requires specification and schematic)
- Part programming (list manufacturer's part number)
- Boundary Scan testing
- FEA (finite element analysis)
- Strain gauge testing (CheckSum automatically quotes this feature if the board has BGA's)

## Acceptable CAD Formats

| CAD System | File Extension | Format |
|---|---|---|
| Accel EDA, Tango | .PCB | ASCII |

| | | |
|---|---|---|
| Allegro | .PIN | ASCII |
| Allegro-Cadence | .BBN | ASCII |
| Calay | .PCB | ASCII |
| Cadnetix | .SCI, .TPT & . NET | ASCII |
| EE Designer | .ALA | ASCII |
| IBM CBDS BNR5 | .ARC (.BNR) | ASCII |
| Mentor | .NET, .CMP, .PRT, .WIR | ASII |
| OrCAD 386 | .BD1 | ASCII |
| OrCAD | .MIN | ASCII |
| PCAD | .PDF | ASCII |
| Protel | .PCB | ASCII |
| SCICARDS | .DAT (.CII) | ASCII |
| Zuken Redac Cadstar | .CDI | ASCII |
| Zuken Cadstar, Visula | .PAF | ASCII |

If you have a CAD system other than those listed above then the files provided to CheckSum must contain the following information in ASCII format plus the Gerber layer files must also be included:
1) Component designator and pin number.
2) Node name or node number for each component pin.
3) X-Y locations of all component pins

## Optimum CAD Formats

| CAD System | File Extension | Format |
|---|---|---|
| Altium (Valor) | .ODB or .ZIP | ASCII |
| Cadence / Valid Allegro | .PAD, .BRD, .SYM & .RTE | ASCII |
| Fabmaster (FATF file) | .FAB | ASCII |
| GenCAD | .CAD | ASCII |
| IPC 356 | .IPC | ASCII |
| Mentor | .NEU | ASCII |
| PADS or PADS PERFORM | .ASC | ASCII |

When above optimum data is supplied, CheckSum can provide testability analysis, guaranteed price quotes, and a discount is built in to the fixture project price.

# Requirements for Fixture Development

| Board Documentation | | |
|---|---|---|
| Item | Preferred Format | Description |
| Schematic | .PDF | CheckSum uses the PDF schematic to provide an electronically annotated document showing all probe numbers on the schematic for future debugging needs. CheckSum can create a PDF schematic from other formats including DXF and DWG, but any schematic in non-PDF formats is by definition, not searchable. Non-searchable PDF's will result in extra charges for fixture development. |
| Panelization Data | .DXF | X/Y offset information between boards in the panel. This can be supplied in one of two ways: panel drawing or panelized gerber files. The information must include reference from tooling holes in panel rails to a drillable hole in the single boards.<br>Note: If the panel contains "mirrored" boards, a drawing must show XY offset from the exact same point within the board outline that can be related to the board CAD or gerber data. |
| BOM | .XLS or .TXT | CheckSum requires a BOM with reference designators and part values for all parts to automate the part value entry. Projects with BOMs in the listed formats will be subject to additional charges. |
| Gerber Files | Varies | The drill files contain the XY location of the holes to be drilled in the test fixture. Full CAD data can substitute for gerber. |
| Net List | ASCII | This file contains the board interconnection data. Without this file, all interconnection information must be entered manually from the schematic. For a simple, one-page (A or B size) schematic, we can work without a net list, but lead time and cost will be greater. For a multiple-page schematic, the net list is required for a fast and accurate quotation |
| Pick & Place | ASCII | Pick and Place is needed, but may be contained in the Net List. Check your CAD data outputs to confirm whether or not Pick and Place data is included or not. |
| Functional Test Procedure | Required for functional test quotations. The test procedure must be a bench verified step-by-step listing of the requested functional tests, testable using CheckSum equipment. A factory test specification is not acceptable as a substitute. | |

| ISP Device Documentation | | |
|---|---|---|
| Item | Preferred Format | Description |
| Data Sheets | .PDF | Data Sheets describe the operation of devices installed on the circuit board. If not provided by customer, must be available on the manufacturer website. |
| ISP Files | Varies | In System Programming files allows test to be developed that program ISP capable PLDs and FLASH memory devices. |

| Sample Boards | |
|---|---|
| Item | Description |
| Assembled Board | At least ONE known good assembled unit sample should be provided for ICT, while a minimum of FIVE sample boards are required for ISP and functional testing. The board(s) should be mechanically and electrically correct and IDENTICAL to other documentation provided. If panelized boards are to be tested, then complete panelized known good boards |

| | |
|---|---|
| | should be provided. The board(s) are used for fixture layout and debug of both the test program and the fixture.<br>Note: The more known good boards provided, the more statistically accurate the test program. |
| Bare Board | For panelized projects, a bare panel board and individual loaded boards can take the place of a panelized loaded board, provided the individual loaded boards have tooling holes present. In these instances CheckSum will ask the customer to sign a waiver as we will be unable to verify all locations of the test program simultaneously. |

# Example of Data Formats

| Bill of Materials | | | | | | | |
|---|---|---|---|---|---|---|---|
| Item | Qty | Reference | Description | MFG #1 | MFG #1 Part Number | MFG # 2 | MFG #2 Part Number |
| 26 | 1 | C24 | CAP, ALUM, ELECT, 330uF, 25V | Panasonic | EEV-KF1E33IP | | |
| 27 | 1 | C21 | CAP, ALUM, ELECT, 47uF, 35V | Panasonic | EEV-FK1V470P | | |
| 16 | 2 | C1, C2 | CAP, CER, NPO, 33pF, 50V, 5%, 0603 | Panasonic | ECJ-1VC1H330J | AVX | 06035A330JAT2A |
| 22 | 3 | C23, C28, C29, | CAP, CERAMIC, 0.1uF, X7R, 50V, 10%, 1206 | AVX | 12065C104KAT2A | | |
| 25 | 1 | C31 | CAP, CERAMIC, 1uF, X7R, 16V, 10%, 1206 | AVX | 1206CY105KATME | | |
| 1 | 3 | C3, C17, C33 | CAP, CERAMIC, X7R, .001uF, 50V, 10%, 0603 | Panasonic | 06031C102JA76A | AVX | 06035C102KAT2A |

| Netlist | | | |
|---|---|---|---|
| *SIG +5V | | | |
| U2.30.U | C3.1.U | C39.1.U | LED1.A.U |
| R1.2.U | C49.1.U | R15.2.U | R4.2.U |
| R3.2.U | R51.2.U | R44.2.U | R65.2.U |
| R52.2.U | R53.2.U | R86.2.U | C51.1.U |
| D16.6.2.U | D11.2.U | L2.2.U | R33.2.U |
| D14.2.U | | | |
| *SIG+12V | | | |
| H600.1.U | U12.8.U | H601.1.U | H602.1.U |
| C16.1.U | C40.1.U | L3.2.U | Q1.E.U |
| R29.2.U | R9.2.U | C44.1.U | C43.1.U |
| U6.1.U | | | |

| *SIG +15V | | | |
|---|---|---|---|
| C34.1.U | C41.1.U | C14.1.U | U5.8.U |
| L5.2.U | C45.1.U | U6.8.U | |

| Gerber |
|---|
| *<br>G04 Mass Parameters ***<br>*<br>G04 Image ***<br>*<br>%MOIN*%<br>%IPPOS*%<br>%ASAXBY*%<br>G74*%FSLAN2X34Y34*%<br>*<br>G04 Aperture Definitions ***<br>*<br>%ADD10C,0.0500X0.0250*%<br>%ADD11R,0.1100X0.0400*%<br>*<br>G04 Plot Data ***<br>*<br>G54D25*<br>G01X0051625Y0019000D02*<br>Y0016750D01*<br>X0024125Y-0003750D02*<br>X0021375D01*<br>X0018625D01* |

| Pick and Place | | | | | | |
|---|---|---|---|---|---|---|
| Designator | Comment | Mid X | Mid Y | Layer | Rotation | Footprint |
| C100 | CP06-0550-1111 | 1728MIL | 150MIL | T | 360 | CAP_COIN_HORZ |
| C101 | CP51-2625-6104 | 5700MIL | 1475MIL | T | 0 | 603 |
| C103 | CP51-0411-6226 | 3775MIL | 25MIL | T | 90 | 1210 |
| C105 | CP55-0960-0746 | 4625MIL | 1900MIL | T | 180 | 3528 |
| C108 | CP51-2625-6104 | 775MIL | 875MIL | T | 90 | 603 |
| C11 | CP51-2625-6104 | 5700MIL | 1050MIL | T | 0 | 609 |
| C112 | CP51-2651-1680 | 475MIL | 850MIL | T | 0 | 603 |
| C114 | CP51-0251-1221 | 475MIL | 50MIL | T | 270 | 805 |
| C115 | CP51-0251-1221 | 475MIL | -125MIL | T | 90 | 805 |