IC Opens/Shorts Testing

Test Philosophy

The tester is used to test an IC for any opens and/or shorts on any IC connection (pin/BGA). The test of the IC is intended to insure that all common pins are connected to the same network of pins, independent pins make a connection to the die, and there are no shorted pins. The continuity test verifies the common pins are connected and that no pins are shorted. Additional tests are used to insure all the independent pins make a connection to the die.

The typical test to insure all the independent pins make a connection to the die is some type of impedance test from the independent pin to another network or pin.

The tester does not perform parametric testing of the IC. The stimulus and measurements are limited to detecting opens, shorts, and some impedance testing using low-voltage signals. The IC is not powered-on during any tests.

The load board connects each pin to a unique test point. For this document, a pin and a test point are equivalent.

A typical test system setup includes:

Windows PC and monitor/keyboard/mouse
Industrial chassis with CheckSum 200 test point modules with four 50-pin cables each
Test Fixture with a vacuum on/off slide-valve
Other items needed that are typically provided from other sources
Load board with IC socket
IC Test Program

Help (test system reference)

The test system manual (PDF file on the CheckSum CD) and the test system software, Help should be used for reference. The Help provides the most efficient method to find the topics of interest.

Testing Methods

Continuity Test

The test system allows you to test the IC for common-pin opens and for a short-circuit between any pins with a single CONTinuity test step. Although the network of connection data can be manually entered, this data is usually self-learned by the System from a known-good component. See the additional information labeled “Continuity Testing for Opens & Shorts”.

IC Test & IC Test Range setup

The System tests for the presence and orientation of the diodes that are present at all of the pins of the IC. These diodes are present to protect the input and output pins from electrostatic discharge by clamping the input voltage between the more positive supply voltage (e.g., VCC) and the more negative supply voltage (e.g., GND). The IC test range setup is used to limit the pins to be tested primarily for the self-learn of a known good IC.

Resistance Test

The test system provides resistance measurement in decade ranges using a constant current source with decade ranges from 0.1µA to 10mA. The measured value is displayed in ohms.

A resistance measurement can be accomplished in several unique methods; 2-wire, 4-wire, 6-wire plus one test point (pin) to a set of other specified pins or from one-pin to all others.

Diode Test

The test system provides diode breakdown measurement in decade ranges using a constant current source with decade ranges from 0.1µA to 10mA. The measured value is displayed as volts.

A diode measurement can be accomplished in several unique methods; 2-wire, 4-wire, 6-wire plus one test point (pin) to a set of other specified pins or from one-pin to all others.

Comparison of Tests

Generation

The different methods to test the IC have unique characteristics for program generation and for diagnostics. For example, the CONT and ICs tests are very simple to create tests, can self-learn the expected results from a known good part or download from a file, and execute reasonably fast. These two tests used in combination provide nearly 100% coverage for most ICs. The resistance and diode tests need to be specified for each separate pin.

Failures

When a failure is detected, the CONT and ICs tests provide the pin failure referenced by name but do not provide the actual measured resistance or voltage. Using the editor features, this information is available to observe these values however the normal test results data that can be saved with each test does not provide these values.

When a resistance or diode test detects a failure, the measured value is available to be displayed and the normal test results data that can be saved with each test does provide these values.

Mapping the IC Pins to the test system resources (test points)

Entering the name and function of each IC connection (pin/ball)

One essential task when creating a test program is to have the test point numbers reference a pin by name. A good pin name includes its function such as power (VCC), ground (GND), other (TCLK), or IO in the leading part of the name. This makes diagnostics and program generation easier.

Example test point names for a BGA IC

The pin names are Row+Column name/numbers followed by the IC pin function:

P10 VCCO_6
F3 IO_L24P_7
D3 TDI
A1 GND
A2 VCCAUX
A3 DXP
A8 IO_L37P_0
C2 IO_L01N_7/VRP_7
E4 IO_L03N_7
H11 GND
R10 VCCO_6

Note that the pin names should be unique. Even the numerous ground pins will be uniquely named with a leading Row+Column pin identifier.

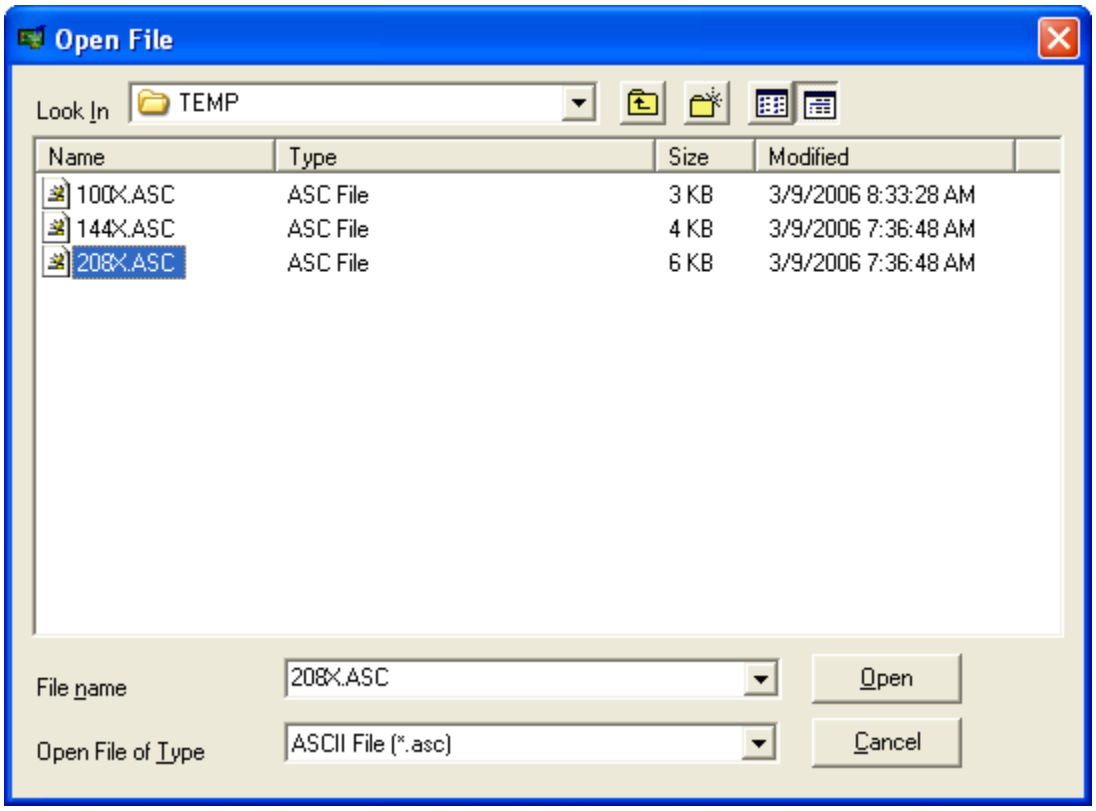
This information will become part of the IC test program. You can enter this information using the test system program editor. You may find this task easier to do with other software tools to create a file with the necessary information and then import (append the file) the file contents into the test program. This saves time and reduces typing errors.

Entering the pin names

See the test system reference section “Assigning Point Names” for manual entry. The editor menu *Setup* > *Fixture Test Points (or Setup* > *Connection Information)* is used to open this window for name entry.

To import this information into a test program, a file needs to be created. This file needs to be in text file format. If you select the file-name extension ASC, the test system will recognize the file for import.

Select the editor menu item *File* > *Append . . .* and the Open File dialog window appears. The *Open File of Type* field **ASCII File (*.asc)** displays only the files with the extension **.ASC** therefore the recommended file name has this extension, such as *filename***.ASC**.



After you press Open, the dialog close and the display will appear unchanged. Use the editor menu *Setup* > *Fixture Test Points (or Setup* > *Connection Information)* to open the connection information window to review the Append process and the names that were imported (Appended).

The contents of the file should be a comma-separated list with the first line “Pin Names:”, such as:

Pin Names:

Test Point Number, IC_Pin_Number_1 IC_Pin_1_Name
Test Point Number, IC_Pin_Number_2 IC_Pin_2_Name
. . . . . .
Test Point Number, IC_Pin_Number_last IC_Pin_last_Name

For example, for a typical load board, each DUT pin is connected to a unique test point:

DUT Pin	Test Point
P10	52
F3	71
D3	77
A1	79
A2	180
A3	289
A8	321
C2	379
E4	391
H11	395
R10	400

Assuming the IC pin names (unique to the IC) are:

DUT Pin	Pin Name
P10	VCCO_6
F3	IO_L24P_7
D3	TDI
A1	GND
A2	VCCAUX
A3	DXP
A8	IO_L37P_0
C2	IO_L01N_7/VRP_7
E4	IO_L03N_7
H11	GND
R10	VCCO_6

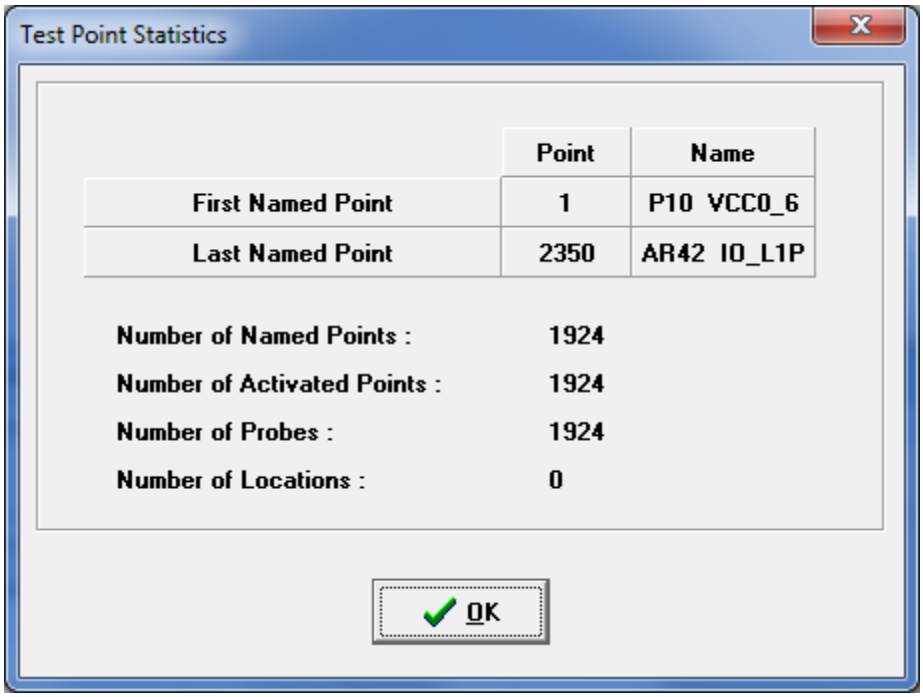
Therefore the text file (for example, DUT123.ASC) to be created should contain:

Pin Names:

52, P10 VCCO_6
71, F3 IO_L24P_7
77, D3 TDI
79, A1 GND
180, A2 VCCAUX
289, A3 DXP
321, A8 IO_L37P_0
379, C2 IO_L01N_7/VRP_7
391, E4 IO_L03N_7
395, H11 GND
400, R10 VCCO_6

Note that the test point numbers can be in any order. They do not need to be sequential or ascending in the file.

After the names have been entered or imported, use the editor menu *Setup > Fixture Test Points > Tools > Statistics* (or *Setup > Connection Information > Point > Statistics)* to open the *Statistics* window and review this to verify the information:



Check the information in this window to verify your expectations. In the above, assuming each test point is connected to a “Named Point”, this would indicate a 100 pin IC. The other information should be verified and match the DUT specifications.

Also make sure there are no duplicate names. Use the editor menu *Setup > Fixture Test Points > Tools > Find Duplicate Names* (or *Setup > Connection Information > Point > Find Duplicate Names)* to check this.

Creating a new test program and entering the test steps

To create a new test program, press the F2 function key or click on the startup window button labeled **Edit Test**. This will open the test program editor window. If no program has been loaded or edited yet, select the **Blank Test Program** button.

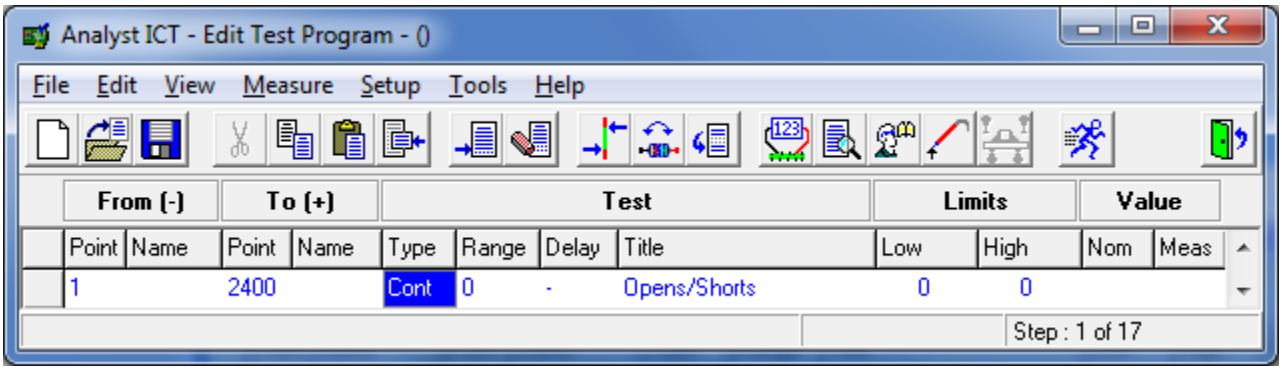
To insert a new test step, press the PC keyboard **Insert** key. See the test system reference section “Edit Test Program Screen”. Once a test step has been entered, use the F1 function key or select the Help menu item *Contents* to access the help information for the test step.

As you enter the test program information, take a moment to **Save** your work from time to time. Press the icon for the diskette or use the editor menu item *File > Save*. The first time you save the file you will need to enter the file name. Select an appropriate file name to match the IC (DUT).

Learn a known-good IC (DUT)

Assuming the test system is connected properly, an IC (DUT) is installed in the load-board socket and every pin has a name follow these steps:

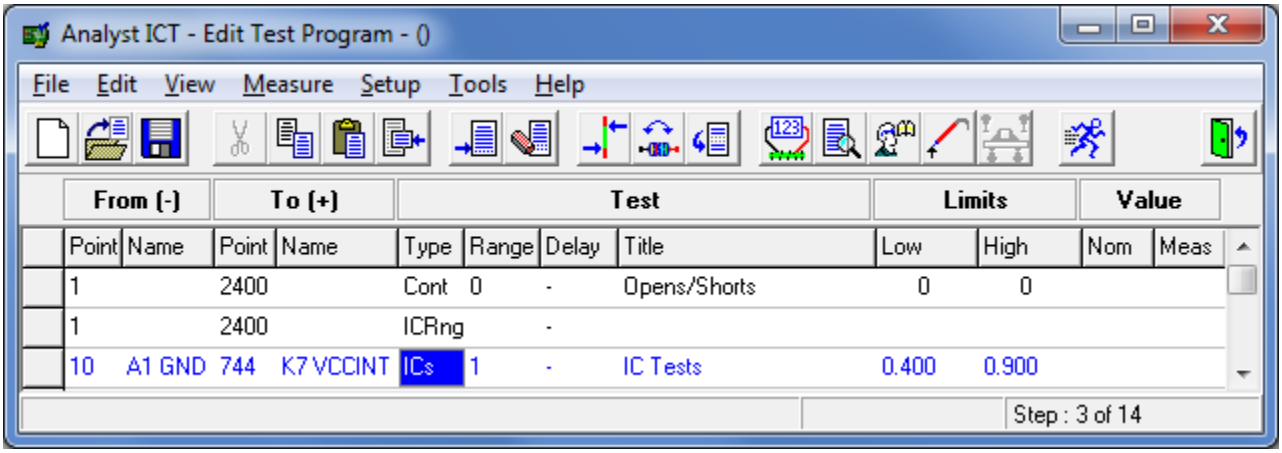
1. Press the Insert key and enter the **Cont** (for continuity) test step.
2. Set the From (-) Point to the *First Named Point* (lowest test point number) shown in the Connection Statistics.
3. Set the To (+) Point to the *Last Named Point* (highest test point number) shown in the Connection Statistics.
4. The previous two steps bound the Continuity test to only the test points of interest and will minimize the test time for this test step.



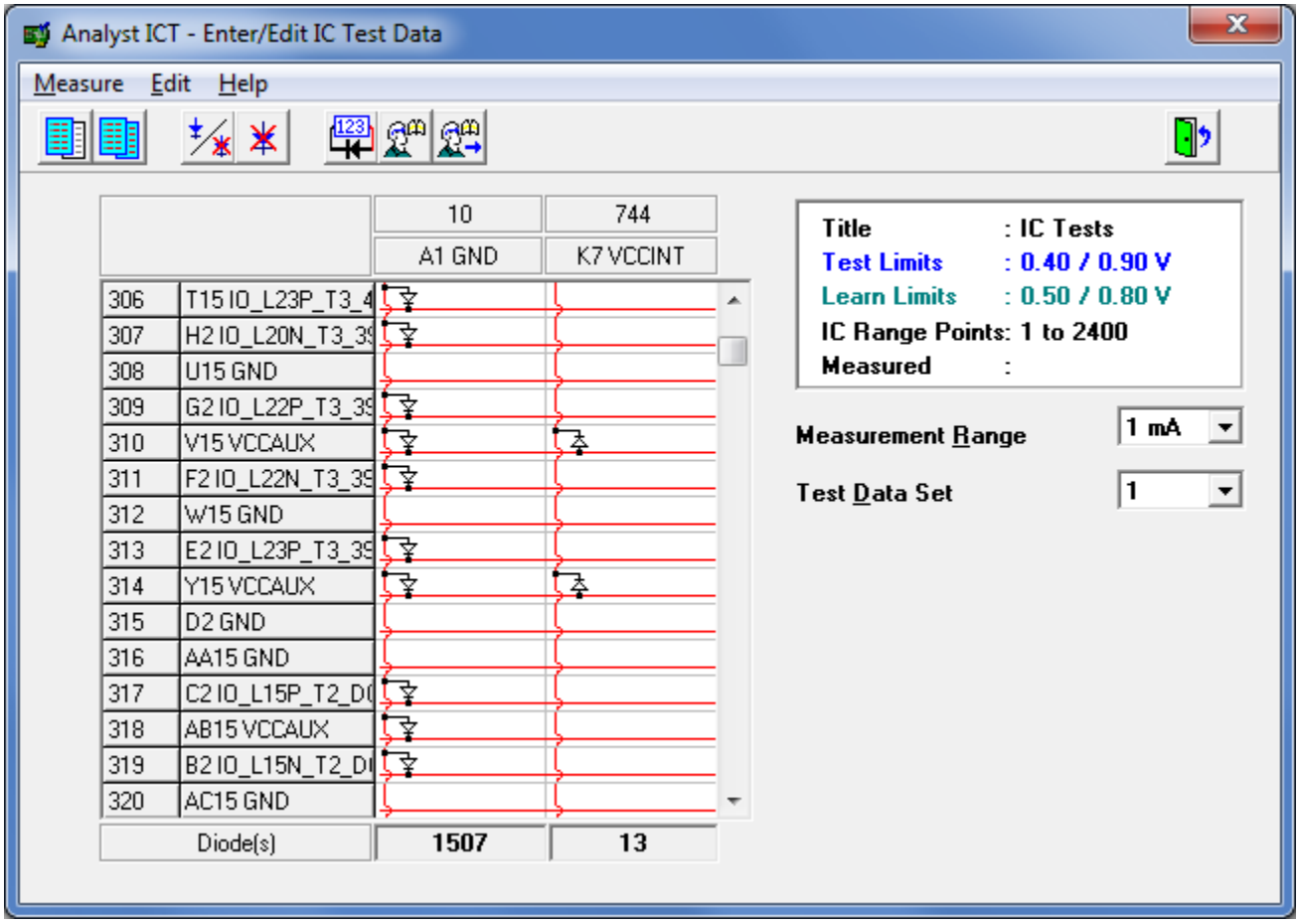
5. Next, press the F6 function key, or select the edit test program menu item *Measure* > *Step Analysis*. See the test system reference section “Measure Menu”.
6. Press the F5 function key or select the menu item *Measure* > *Self-Learn All*
   The self-learn will execute and provide a summary of the learned results. The Total Networks should equal the connected IC pins (PWR pins are 1, GND pins are another etc). The separate I/O pins are not counted (a network requires 2 or more pins to be connected).
7. Review each network to verify that the expected number and name of pins are included and excluded appropriately.
8. Press the green door icon or select the menu item *Measure* > *Exit* to store the continuity results and return to the main editor window.
9. Save your work now.

Now using the ICs test the second part of the test will be created.

1. Press the Insert key and enter the **ICRng** test step.
2. Set the From (-) Point to the *First Named Point* (lowest test point number) shown in the Connection Statistics.
3. Set the To (+) Point to the *Last Named Point* (highest test point number) shown in the Connection Statistics.
4. Press the F3 function key or select the menu item *Measure* > *Make Measurement* to execute this step. This step bounds the **ICs** test to only the test points of interest and will minimize the test time for the next test step (**ICs**).
5. Press the Insert key and enter the **ICs** test step.
6. The 'From (-)' and 'To (+)' test point columns indicate the power supply pins that you will be measuring from each point for diode presence. For the From (-) Point, enter the test point number of the more negative supply for the IC (e.g., GND). For the To (+) Point, enter the test point number for the more positive test point (e.g., VCC).



7. Next, press the F6 function key or select the edit test program menu item *Measure* > *Step Analysis* See the test system three reference sections “Entering the ICs Test Step”, “The Enter/Edit IC Test Data Screen” and “Learning the ICs Map”.
8. Be sure that the IC Range Points match the points specified in the **ICRng** step otherwise you may wait while the test system learns all the test points in the entire test system rather than just the limited number of test points connected to the DUT. See step 4 in this sequence.
9. Press the F5 function key or select the menu item *Measure* > *Self-Learn All*
   The self-learn will execute and update the number of diodes detected from the two supplies listed at the top of the two columns.



10. Press the F3 function key or select the menu item *Measure* > *Measure All* to verify the test appears to work without any failures.
11. Note the number of diodes in the count at the bottom of the two columns.
12. Press the green door icon or select the menu item *Measure* > *Exit* to store the continuity (data base) results and return to the main editor window.
13. Save your work now.

You can add some useful documentation to the test and help the operator use this test.

1. Select the editor menu item *Setup* > *Assembly Name* and enter the DUT name.
2. Select the editor menu item *Setup* > *Operator Instructions Setup* and enter the instructions for the operator to install an IC (DUT) into the IC socket, lock the socket handle, and press any key to run the test.
3. Press the green door icon or select the menu item *Measure* > *Exit* to store the continuity results and return to the main editor window.
4. Save your work now.

If a Resistance or Diode test is preferred, enter the test point pins of interest. On each test step, press the F6 function key or select the edit test program menu item *Measure* > *Step Analysis* to setup any special measurement features. See the test system three reference sections labeled "Entering Resistor, Inductor and Capacitor Tests", "Diode, LED and Zener Testing", and "Measurement Analysis". Each pin will be tested separately and in addition to the tested pins, the failure results will indicate the measured value, ohms, for the resistance tests and volts, for the diode tests. For advanced reading, see the test system reference sections labeled "Choosing a Range/Function", "External Sense", "Guarding", and "Measuring One Point to Many Points".

To make test program entry easier, when testing the I/O pins with a resistance or diode test, the special "one pin to all others" measurement can be used. The concept is to force a current into each I/O pin and connect, via low-resistance solid-state switches, all the other pins together. This eliminates the task of selecting the pin pairs for each I/O pin. If this selection is easy to do, then by all means, proceed with setup you prefer. For advanced reading, see the test system reference section "Measuring One Point to Many Points".

The resistance and diode test steps have a Title field that is normally used to indicate the component tested by this test step. Since the test point names uniquely identify the pin tested, entering any information into the Title field is optional.

Importing the Continuity (Opens/Shorts Test) Data

An alternative to using a known-good part to learn the continuity and/or ICs database is to use a file to import this information.

There are definite advantages with the import method. First, you do not need a known-good part. Second, the data is in a file which does not rely on the tester, test setup, or the part.

Just as the pin names can be defined in a file, the continuity data can be defined in a separate file or the same file as the pin names and ICs database.

The format for the continuity can be defined in two ways, with pin numbers or pin names. To use the pin names, the pin name data must be present in the file or previously defined in the test program.

For example, if the IC has two power pins in a net and three ground pins in another net, the continuity file contents would need two sections for the two nets. A blank line separates the two nets.
Assume the device power pins (V3P3) are connected to test point numbers 2 and 14 and the ground pins (GND) are connected to test point numbers 11, 21 and 22.

The continuity could be specified in a file using the test point numbers as such:

```
Continuity:

2() to 14()

11() to 21()
21() to 22()
```

Notes: Use a Space character (one or more is ok), not a Tab character between the items. The blank line below `2()` specifies the start of the next net.

The pin names can be included in the file, or previously defined in the test program. For example, to define the pin names and the continuity in one file, the contents could be:

```
Pin Names:

   2, A12 V3P3
  11, R12 GND
  14, B6 V3P3
  21, H19 GND
  22, K7 GND

Continuity:

  (A12 V3P3) to (B6 V3P3)

  (R12 GND) to (H19 GND)
  (R12 GND) to (K7 GND)
```

Notes: Use a Space character (one or more is ok), not a Tab character between the items. The blank line below `(A12 V3P3)` specifies the start of the next net.

Importing the ICs Data

The pin names can be included in the file, or previously defined in the test program. For example, to define the pin names and the ICs test database in one file, the contents could be:

```
Pin Names:

   2, A12 V3P3
   5, J2 IO_Data_1
  11, R12 GND
  12, J2 IO_Data_8
  14, B6 V3P3
  21, H19 GND
  22, K7 GND
 135, J2 IO_Data_3
 144, J2 IO_Data_2
 249, J2 IO_Data_4
 254, J2 IO_Data_7
 299, J2 IO_Data_6
 310, J2 IO_Data_5

IC Tests:

Range 1 from ~J2 IO_Data_1, ~J2 IO_Data_8, ~J2 IO_Data_3, ~J2 IO_Data_2
Range 1 from ~J2 IO_Data_4, ~J2 IO_Data_7, ~J2 IO_Data_6, ~J2 IO_Data_5
Range 1 to   ~J2 IO_Data_1, ~J2 IO_Data_8, ~J2 IO_Data_3, ~J2 IO_Data_2
Range 1 to   ~J2 IO_Data_4, ~J2 IO_Data_7.
```

If the pins named are not included, or pre-defined, in the test program, the pin numbers can be used to specify the diodes for the ICs test:

```
IC Tests:

Range 1 from 5, 12, 135, 144, 249, 254, 299, 310
Range 1 to   5, 12, 135, 144, 249, 254
```

Notes: Use a Space character (one or more is ok), not a Tab character between the items. The "from" section lists the diodes between the From (-) pin to the specified pin. The "to" section lists the diodes between specified pin and the To (+) pin.

The Range number identifies the ICs test data set. Up to four (4) data sets can be defined in a test program. Each ICs test step specifies the From (-) pin and the To (+) pin.

The following is an example of a section of a file with two (2) ICs test steps (Range 1 and Range 2) where the pins names have been predefined:

```
IC Tests:

Range 1 from ~J2 IO_Data_1, ~J2 IO_Data_8, ~J2 IO_Data_3, ~J2 IO_Data_2
Range 1 from ~J2 IO_Data_4, ~J2 IO_Data_7, ~J2 IO_Data_6, ~J2 IO_Data_5
Range 1 to   ~J2 IO_Data_1, ~J2 IO_Data_8, ~J2 IO_Data_3, ~J2 IO_Data_2
Range 1 to   ~J2 IO_Data_4, ~J2 IO_Data_7

Range 2 from ~J2 IO_Data_1, ~J2 IO_Data_8, ~J2 IO_Data_3, ~J2 IO_Data_2
Range 2 from ~J2 IO_Data_4, ~J2 IO_Data_7, ~J2 IO_Data_6, ~J2 IO_Data_5
Range 2 to   ~J2 IO_Data_1, ~J2 IO_Data_8, ~J2 IO_Data_2, ~J2 IO_Data_4
Range 2 to   ~J2 IO_Data_5
```

Insuring 100% Test Coverage

What 100 % coverage means

The goal is to verify that every pin of the DUT in connected to the die of the IC. If the Continuity test insures 43 of the pins are connected to the die and the ICs test, or Resistance, or Diode tests, insure the remaining 57 pins are connected to the die you have 100% connectivity tested.

How to verify each pin is correct

Now you can print the test program to a file or paper and review this information. One simple method is to review the CONT learned connections and summarize these results. For example, if the CONT test shows 3 Total Networks and 22 Connected Points, then you should verify that this matches the IC. Also, each named point should be correct for each network. For example, are all of the GND pins on this network named "pin_number followed by GND"? Does the number of GND pins match the IC specification?

The task is to insure each IC pin is tested. By counting and verifying the pins listed in the CONT test and the pins tested in the ICs test, a complete list of the IC pins can be verified. There is often some overlap is the test coverage with continuity and ICs test steps. You must insure each pin of the IC is tested at least once.

What is not verified

If the continuity and ICs test does not include an IC pin, then this pin needs to be tested another way. Some ICs have a temperature diode that is connected between two pins. Add a diode test for these two pins. Some ICs have pins that are not defined or that the function may change. Add a remark to the test program to alert anyone else examining the test program that these pins are not tested if this is the case.

As mentioned previously, the power-on function of the IC is not tested only the connections from the pins to the die. Since the connection is tested as an impedance, if two identical types of connections were swapped (highly unlikely event), the test would still pass however the IC would fail function test. If the connection has an impedance which is current-dependent, the IC test may pass but when the IC is powered-on, a higher-current may cause a voltage drop that causes the IC to fail function test.

Running the Test

Execute the test

From the startup window press the F1 function key or click on the button “Run Test”. If no test program has been opened, an Open File dialog window will prompt for the test program to be selected. If a test program has been loaded, the system will confirm that this is the test program to be executed.

From the editor, either exit to the startup window as previously described or press the “running man” toolbar button.

Setup the test

The test window includes several setups. See the test system operation reference sections beginning with “Testing an Assembly”. One particularly useful menu item is the Test window menu item *Test > Halt on Fail*. When checked, any failure will stop the test program and allow the operator to take some action, if necessary. For any automated handler setup, be sure to uncheck this item.

Diagnostics - Understanding the Failure Messages

Continuity test failures

If the continuity test fails, there are two possibilities; an OPEN circuit or a SHORT circuit. The OPEN circuit failure message indicates the pin that is not connected to the network as expected. The SHORT circuit failure message indicates the pin that is connected to another network. It is possible that the failure is due to an impedance that is not really a short or an open. The Continuity test can be setup with different thresholds for detecting Opens and Shorts. See the additional information labeled “Continuity Testing for Opens & Shorts”.

Depending on where the failure is detected, you may receive multiple failures that are essentially the same failure. When a very large network (such as 181 nodes) has a short to another very large network (such as 49 nodes), the exact number of failures is not very meaningful. How many shorts should the system report between these two nets? One answer would be 181*49 or 8,869 failures. This seems a bit to verbose for useful work. The system will report failures based on the 200 test point modules; for example one failure may be reported in each range of 200 test points. There are other interesting rules for the failure reports but they are even more complicated.

A typical SHORT failure display will show:

```
52        400        Cont    0   Opens/Shorts      0      0       1 *
      Short: N8 IO_L86P_7 (208)  to  M8 IO_L56P_7 (209)
```

Note: The 1 * at the end of the test step line indicates there is one failure for this test step. The next line specifies the failure details. Two pins that are not connected in the Continuity data base have a SHORT circuit. The reason for the failure is likely due to a SHORT circuit inside, or external to, the IC.

A typical OPEN failure display will show:

```
52        400        Cont    0   Opens/Shorts      0      0       1 *
      Open: A1 GND  (206)   to  H4 GND (269)
```

Note: The 1 * at the end of the test step line indicates there is one failure for this test step. The next line specifies the failure details. Two pins that are in the same network (connected in the Continuity data base) have an OPEN circuit. The reason for the failure is likely due to an OPEN circuit inside, or external to, the IC.

ICs test failure

The only failure for the ICs test is a measured value that is not within the test limits. The ICs data base (i.e., learned diode array from a known good IC) for the ICs test indicates diodes in unique locations. During the ICs test, any diode that is “in the data base” that measures a voltage less than, or greater than, the test limits will cause a failure. The failures displayed, and saved in the test results, are the pins involved, not the voltage, such as:

```
206   A1 GND    331 K7 VCCIN     ICs     1     IC Tests   0.400   0.900       2 *
      A1 GND(206) to: F3 IO_L24P_7(155)
      K7 VCCINT(331) to: G3 IO_L34P_7(159)
```

Note: The 2 * at the end of the test step line indicates there were two failures for this test step. The next two lines specify the two failures. Two diodes that were learned from a known good IC are missing or exceed the specified test limits (0.400 volts to 0.900 volts). The reason for the failure is likely due to an OPEN connection inside the IC.

Resistance test

The only failure for the resistance test is a measured value (units are ohms) that is not within the test limits. A typical resistance failure display will show:

206 A1 GND 269 H4 GND Res 12 0.0000 10.000 12.458 *

Note: The * at the end of the test step line indicates that the test failed. The Low Limit of 0.0000 ohms is shown and the High Limit of 10.000 ohms is shown along with the actual measured value of 12.458 ohms.

Resistance O_Rng Note

To enter a value higher than the system can measure, enter **O_Rng**. This high limit value is greater than any normally measured value, and will never cause a High Limit failure. An over-range measurement is shown as **O_Rng** in the measured value.

Diode test

The only failure for the resistance test is a measured value (units are volts) that is not within the test limits. A typical diode failure display will show:

206 A1 GND 257 E4 IO_L0 Diode 2 0.400 0.800 0.388V *

Note: The * at the end of the test step line indicates that the test failed. The Low Limit of 0.400 volts is shown and the High Limit of 0.800 volts is shown along with the actual measured value of 0.388 volts.

Diode O_Rng Note

To enter a value higher than the system can measure, enter **O_Rng**. This high limit value is greater than any normally measured value, and will never cause a High Limit failure. An over-range measurement is shown as **O_Rng** in the measured value.

Find a pin (Probe a Point)

The actual cause of a failure may not be the measurement or the connections to the IC die. The real problem is that the test system is simply not connected to the pin. This can be caused by several possible problems. To insure the test point resource is correctly connected to the IC pin, use the test system capability called “Probe a Point”. This “Probe a Point” capability sets the system into probing mode. The probe needs to be connected to the red banana jack on the back panel of the System Module. In the editor, to in initiate this capability select the menu item *Setup > Connection Information > Point > Probe a Point F3*. Probing can also be turned on and off with the toolbar item that resembles a probe touching a point.

When in probing mode, each time the probe touches a test point, the test point moves to the middle of the screen. Probing stays active until Probe a Point is selected again to toggle it off. Use this feature to verify the test point is correctly connected to the IC pin. If the connection appears to be incorrect, use the probe to track the test point connections from the 50-pin cable to the fixture spring-probe, to the load-board connector, and finally to the IC socket. Eliminate the good connections and this will isolate the incorrect, or faulty, connection. If you can touch the IC pin, you can verify the test point number that is connected to this IC pin.

Other considerations

Save the results for each test

The test results can be stored for future analysis. At the startup window, select the "**Configure System**" button or press the F4 function key and then click the tab at the top labeled "**Environment**". Now, click the "**Configure Reporting**" button of the Environment page, to obtain the Configure Reporting window. This window is used to specify report formats, SPC logging and automatic reporting for the System.

Click the **SPC Logging** tab to configure the system data logging setup. Check the "Statistics Data Logged" entry to turn-on saving test results. Statistics Data Logged is used to turn on or off SPC data logging and specify how much data is saved from testing for SPC analysis. If the box is not checked, no test results data is saved. If it is turned on (box is checked) 'Summary' information about the test such as pass/fail status, test time, operator, serial number and so on is saved. No detailed test step results are saved unless either the Pass or Fail Results box is checked.

- Passing Results saves detailed information about the test steps that pass
- Failing Results saves detailed information about the test steps that fail.

Most installations that use SPC logging save Fail Results information. This allows you to obtain Production Reports and Pareto Charts. When you are debugging test programs, it is normal to save Pass Results. This allows you to obtain X-Bar/Sigma reports for fine-tuning the test program.

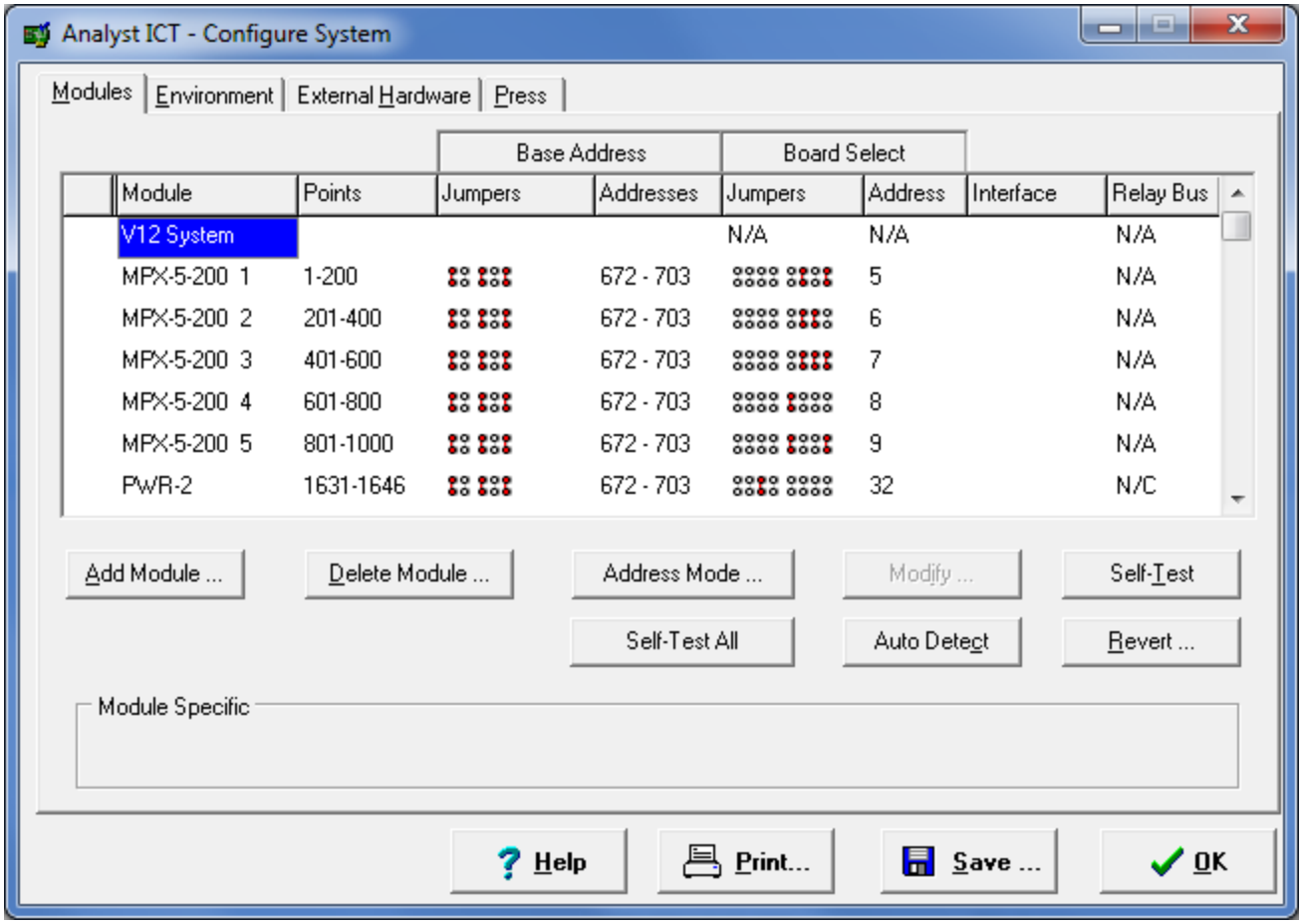
See the test system reference section "Configure Reporting".

Self-test of the test system

If the test system does not seem to be functioning as expected, the built-in system self-test capability can be used to verify the test system. Since the test system is configured with several modules, each module can be tested as needed. See the test system reference section "Built-In Self-Test".

At the startup window, select the "**Configure System**" button or press the F4 function key and then click the tab at the top labeled "**Modules**".

The system self-test should start with the System module (TR-10 or TR-8) and proceed with each of the remaining modules, one at a time. Click to select the module and press the Self-Test button.



When the operator runs the self-test for each MPX module, there are two parts to each MPX self-test.

1. For the first part, you must remove the 50-pin shorting fixture from the end of each cable or the copper plate from the vacuum box (release vacuum).
   The self-test window dialog instructs the operator to "Please remove any shorts to testpoints"

2. For the second part, you must install the 50-pin shorting fixture to the end of each cable or apply vacuum to pull the copper plate down onto the spring-probes.
   The self-test window dialog instructs the operator to "Install shorting fixture to points 1-50" and then 51-100, etc