# IN-CIRCUIT MANUFACTURING DEFECTS ANALYZER (MDA) SYSTEMS FOR HIGH-DENSITY ASSEMBLIES

*Ken Hallmen*
*CheckSum, Inc.*

High-density assemblies may require special methods of access for production test. The traditional access method using a bed-of-nails to contact the component leads, vias and test pads is usually a viable solution. Test coverage using only bed-of-nails for test access can sometimes be inadequate to meet stringent quality standard requirements for some high-density assemblies.

Manufacturing defects analysis (MDA) combined with a vectorless test technique and boundary-scan are complementary test methodologies that can be used together on even the most densely populated assemblies. The test strategy becomes especially intriguing when the approach provides short test times with high fault coverage and low-cost implementation compared to the alternatives.

All three of these test methodologies rely on information that is generally readily available. Many companies are aware of the need for design-for-test (DFT) in the engineering development of virtually every product. The Gerber files, net lists, and schematics with a bill-of-materials provide the necessary information the designers of the production test systems need to do their job. Alternatively even without Gerber or drill files, with a sample assembly, the test points can be optically digitized.

### Fault Spectrum Changes Test Requirements

As the industry moves from through-hole to surface-mount-technology (SMT), the fault spectrum is changing. The test requirements have been changing from finding component failures to finding process faults due to the trend of improvement in component quality. Surface-mount-technology has changed the fault spectrum from mostly shorted components (through-hole technology) to open connections. The other significant faults are missing, misaligned or wrong parts. Solder shorts are still a manufacturing defect in about 12%-15% of the faulty assemblies.

The major thrust for manufacturing defects analysis testing is to detect and remove process related faults. The manufacturing test strategy relies on the assumption that the circuit design is valid. Since the purchasing department is buying only good parts, the remaining problems are soldering related (too little or too much) and accurate placement of the correct components on the printed circuit board.

### In-Circuit, MDA Testing

This test methodology uses a bed-of-nails fixture to access the electrical nets on an assembly. By using programmable source and sense signals plus multi-point guarding, as needed, the components are isolated from each other to allow them to be tested in-circuit. This provides a validation of the manufacturing process such that assemblies that pass have the right components located in the correct place and soldered to the printed circuit board

correctly.  The bed-of-nails fixtures require only one access pin per net using standard, point-to-point wire-wrap wiring.  This reduces the complexity and cost of test fixtures.

Using standard complex-impedance measurements, these MDA tests can all be performed without applying power to the assembly.  This power-off testing eliminates the potential of damaging an assembly due to possible unintentional short-circuits introduced during the manufacturing process.  These unintentional short-circuits occur from PCB etching shorts and solder bridging.

In addition to opens and shorts, an MDA test easily finds all the typical faults for the analog components.  Included in the list of analog components are resistors, capacitors, signal diodes, zener diodes, inductors, transformers, FETs and transistors.  For the digital components, an MDA tester can test the pins of an IC for the presence of protection diodes.

The CAD data for the assembly can be used to create an MDA test program for the assembly.  The net list, component type/name, and value are sufficient to automatically generate the test program.  Typically, the automatically generated MDA test program requires refinement and optimization, however the test program is 70%-80% completed with CAD conversion tools.

### MDA Test Results
One of the powerful features of the MDA test system results is that when a fault is detected, the part is uniquely identified.  Since the parts are being tested in isolation, when a failure is detected, the part reference designator specifies the failing component.  In contrast, functional test failures provide little or no information regarding the actual fault.

### Add Test Probes
A requirement for complete test coverage on an in-circuit MDA test system is access to all the electrical nets (nodes).  Most designs do have the necessary board space, however some assemblies do not have the real estate available to provide access to all the nets.  Single-sided probe access is less expensive however, double-sided (top/bottom) access is routinely used.  If the assembly has space to add test access, a little planning can provide a big payback in the test coverage and cost of developing the test fixture.

*Probe Spacing*
Ideally, boards should be tested with industry-standard 0.100" spring probes.  These low-cost and reliable probes are designed to probe circuit points that are 100-mil (.100") or more apart from center-to-center.  If it is not possible to have the luxury of 0.100" spacing, standard probes are designed for .075" access, .050" access, and even closer spacing is available (see Figure 1).
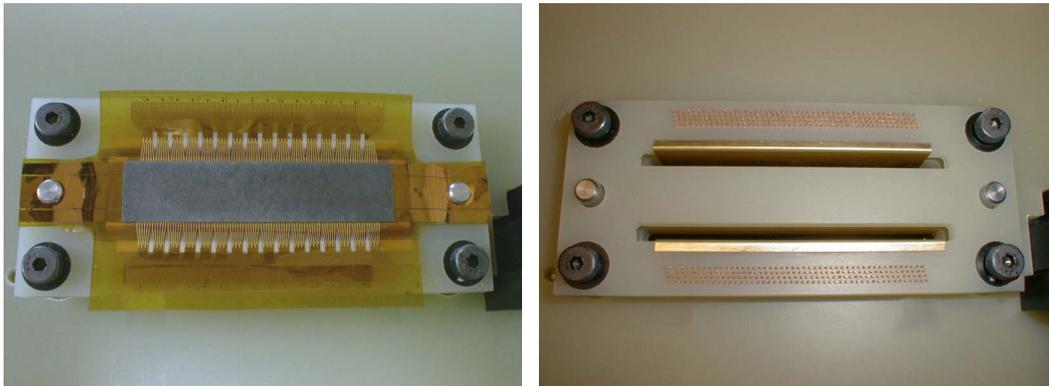
**Figure 1   14-mil Test Point Spacing**

*Probe Targets*

For reliable probing, the probes need to have good targets.  Each probe should contact a target .035" in diameter or larger, ideally .050".  The targets should be as large as possible, when using double-sided probing the top probe targets should be .045" or larger.

The probe target can consist of:
- A test pad, round or square,
- A through-hole with a soldered lead,
- An open through-hole,
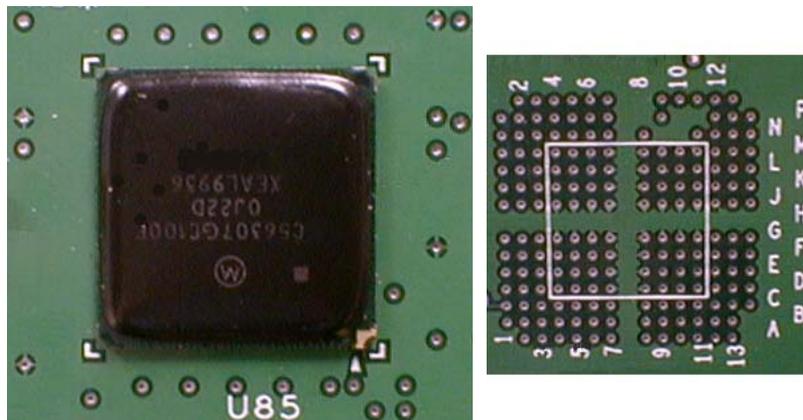- A non-masked via (see Figure 2)



**Figure 2   Via Test Points**

For probing on soldered leads, ensure that the lead trim-length is consistent within plus and minus .030".  Open through-holes should have a relatively small hole diameter so that the probe can contact the edge of the hole.  For standard probing, the hole should be less than .050".

Probing on leads of SMT devices should be avoided.  Because of the variability of the placement and edge geometry, probing can be unreliable on SMT leads.  Also, the probe can press the SMT lead to the pad, causing a bad connection to appear to be good.

*Target Plating and Solder-Resist*

Solder-resist (solder-mask) or conformal coating prevents the probes from making electrical contact, so the probe contact areas must not be covered with either of these materials. Ideally the solder-resist should be removed at least .020" radially from the probing target. This prevents the problem of having the probe contact the solder-mask first, preventing it from contacting the target.

Target surfaces should be gold or solder-coated for best probing. Generally, harder materials are more difficult to obtain a good contact, and have a tendency to dull the probes prematurely.

*Alignment Holes*

Assemblies are accurately positioned on the test fixture with the use of guide pins that mate into tooling holes in the assembly. The assembly should have at least two tooling holes for positioning. These should be as far apart as practical, with the ideal being on two opposite corners.

Tooling hole sizes that work well fall into the range of .125" to .250" diameter. These sizes are easy to accommodate with off-the-shelf guide pins, and are strong enough for use without damage or premature wear. Tolerances between the tooling holes and targets should not exceed ±.002", and probe targets should be at least .175" from the center of the tooling hole.

If the assembly is symmetrical, provisions should be made for a third non-symmetrical hole that is used to keep from installing the assembly onto the fixture with the wrong orientation.

### Vectorless Test

If net access is possible the first easy improvement in fault coverage is to add a test that senses open connections to SMT ICs. This test improves on the MDA IC presence test since it confirms connection between the PCB and the IC using a sensor plate. TestJet, Opens Xpress, and WaveScan are similar "vectorless" technologies that allow digital elements to be tested by sensing signals coupled through the component connections on the PCB to a sensor plate mounted on a test fixture (see Figure 3).



**Figure 3   Sensor Plate Positioned Over an SMT IC**

This technology can also be used to test the polarity of some types of capacitors. Since this test technology relies on the same in-circuit test access, the cost of the related programming and the test fixture is only marginally more due to the addition of the sensor plates.

The stimulus and response for using a "vectorless" technology can be completely automated. Since the component with the sensor plate is a part listed in the net list file, an automated method (self-learn) can be used to apply the stimulus to each of the nets connected to the component and measure the response for each of the leads on the component.

This test technology generally has limited success testing the power and ground pins on the components. The MDA test can identify any short-circuits between nets however an open to the IC power or ground pin would still be undetected even with the MDA and vectorless testing. This limitation can be overcome by implementing boundary-scan testing for assemblies designed with this technology.

### *MDA Plus Boundary-Scan*

If the assembly contains digital components that are IEEE 1149.1 compliant (boundary-scan) and the assembly has been designed for test, a combination of MDA and boundary-scan testing can be used to reduce the nodal access requirement. An assembly designed to use boundary-scan can utilize nets with the boundary-scan chain to test for several potential faults. The boundary-scan path can be used to access the nets without using standard fixture test probes.

Test coverage using boundary-scan testing alone may be limited. This results from the design of the assembly with non-boundary-scan compliant components that can isolate the boundary-scan ICs. All of the standard analog discrete components also need to be tested. The MDA tester can perform this job. Often, the lack of test access and the possibility of using boundary-scan can be used together to maintain high test coverage with fewer physical test probes.

Since boundary-scan is a power-on, functional type of test, it is necessary to perform an MDA test prior to applying power. Since the boundary-scan test can selectively source and measure signals from one boundary-scan IC to another, shorts and opens between the nets can be tested directly. Since the fault spectrum for SMT is dominated with opens circuits, this in-system test improves the fault coverage significantly.

In addition to being able to identify pins with an open connection, missing or incorrect ICs are also detected. Boundary-scan testing can include board-edge connections, cluster testing, and memory cluster testing. Boundary-scan automatic test generators that reduce the time of test development and incorporation of changes are available.

In the example shown in Figure 4, without test access to the nets between the boundary-scan compliant ICs, a short-circuit from an IC net to a power net could potentially damage one or more ICs. Other short circuits to non-compliant ICs may not be detected depending on the drive capability of the ICs involved. The resistor, R1, can be either tested via the standard test access probes or with reduced fault coverage, the connection through the

resistor can be tested.  The value of R1 can be incorrect but if the value is not tested, a test through the part with boundary-scan test vectors may pass however the true, at-speed performance may fail.
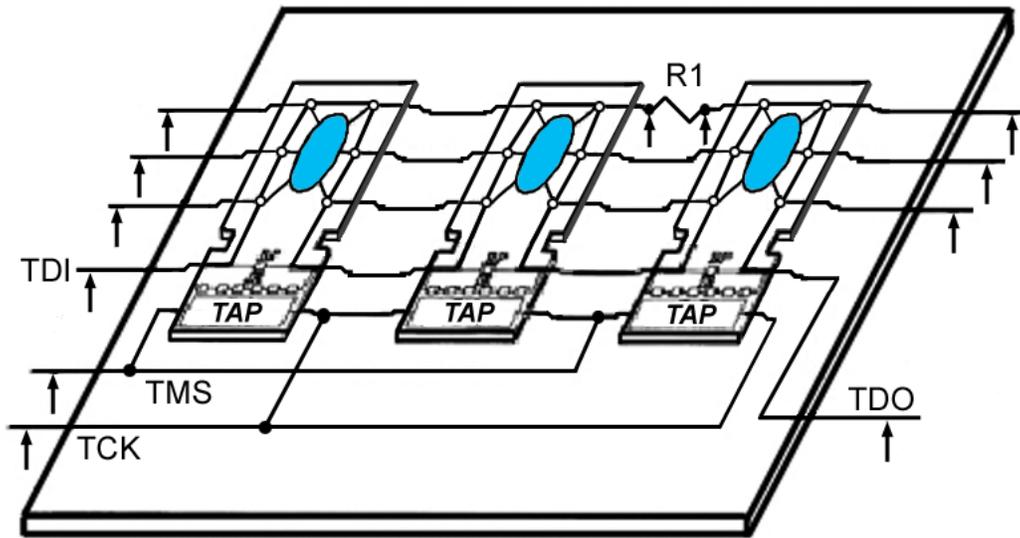


**Figure 4   MDA Plus Boundary-Scan Test Points**

*In-System Programming (ISP)*
Another benefit of using boundary-scan as part of the test strategy is the added capability for in-system programming (ISP).  Several of the manufacturers of FPGA and Flash programmable parts such as Intel, AMD, Altera, and Xilinx have adopted the boundary-scan port as the programming interface for some of their ICs.  After the manufacturing defects have been eliminated, the test system can use the boundary-scan path to download the latest code to the programmable ICs.  The vendors of boundary-scan tools have added capability to decrease the programming time for Flash and PLDs with special hardware and software.

## PC-Based Test Systems
The PC-based test system is the predominate configuration of the vast majority of test systems.  The hardware and software is affordable for almost any manufacturer.  The power and performance continues to increase while the price drops.

The price for low pin count (400) MDA test systems is now under $20 per pin.  This includes the pin electronics, receiver system, computer, statistical process control (SPC) package and CAD conversion tools in a Windows test system software environment.  Adding vectorless test and boundary-scan test capability to an MDA test system increases the overall cost to about $45 per pin.

The ever-increasing performance of the PC platform provides fast test times today and in the future.  Typical test times for the combined MDA test with vectorless and boundary-scan tests are less than 30 seconds.

### Conclusions

The in-circuit, MDA test is recommended to detect and identify all the common manufacturing defects.  Adding vectorless test increases the fault coverage significantly for high-density SMT assemblies.  Adding boundary-scan will further increase the fault coverage and can reduce requirements for test probe access.  The standard in-circuit test fixture provides excellent fault coverage when access to all the electrical nets is available.  On assemblies with limited board space for test probe access, a combination of test probes and boundary-scan can provide almost identical fault coverage with fewer, selected test points.


### *Biography*

Ken Hallmen is the CheckSum Marketing Manager.  He previously held engineering and engineering management positions at Tektronix and the Fluke Corporation.  He graduated from the University of Washington with BSEE and MSEE degrees in electrical engineering and earned an M.B.A. degree from Seattle University.

**CHECKSUM** ✓

**CheckSum, Inc.**
**6120  195th  St.  NE  /  P.O. Box 3279**
**Arlington,  WA  98223**
**Tel   (360)  435 - 5510**
**Fax  (360)  435 - 5535**
*Web Site:  www.checksum.com*

Contact:   **Ken.Hallmen@checksum.com**