Datasheet and User Manual
5200-133
Relay Driver

17 July 2013

Features

The 5200-133 board is a sixteen-line relay driver. This board is constructed with two ULN2803A driver chips. It is capable of sinking 500mA on each output.

Operational Characteristics

I/O Pin Descriptions

Board I/O function is accessed through two 16 pin headers; P1 and P2.

P1 INPUT
16 Pin Header, input 1 through 16

P1 PINOUT

Pin P1-	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
FUNCTION	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN

P2 OUTPUT
16 Pin Header, output 1 through 16

P2 PINOUT

Pin P2-	1	2	3	4	5	6	7	8
FUNCTION	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT

P2 PINOUT cont

Pin P2-	9	10	11	12	13	14	15	16
FUNCTION	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT

P3 & P4 PINOUT

Pin P3- Pin P4-	1	2
FUNCTION	GND	V+ Vclamp

Vclamp limits the "flyback" voltage from relay coils and it should be tied directly to the relay supply.

Truth Table

INPUT	OUTPUT
1	0
0	1

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Output is inverted

Programming Requirements

None

Communication Busses

none

AC DC Requirements

PARAMETER	Min	Typ	MAX	Units	NOTES
Input	0		5	V	TTL input
Vclamp	0		50	V	Match relay operating voltage
Iout			500	mA	Sink each output

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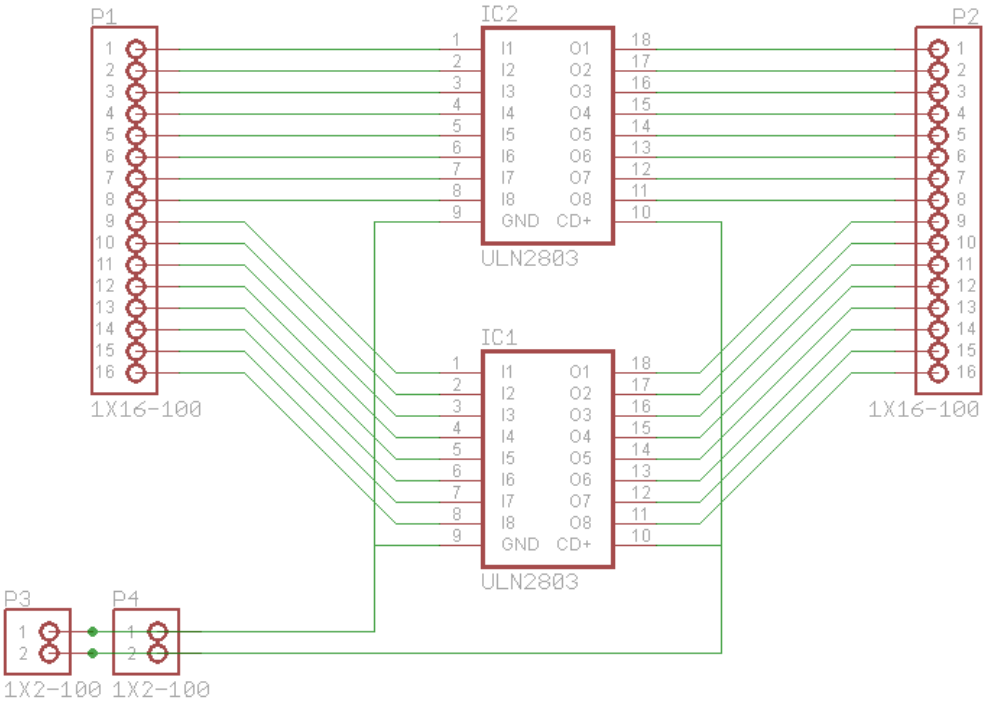
Schematic and Board Layout

Schematic



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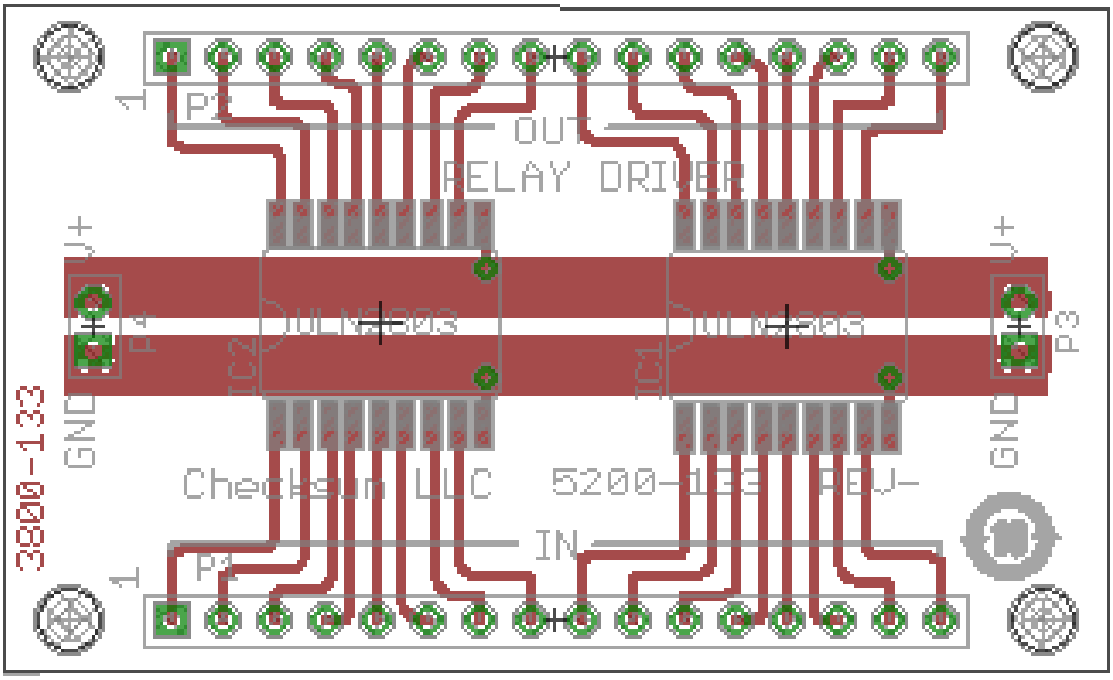
PCB Layout



Board Dimensions & Mounting

Mounting hole diameter is 0.126 inch (3.2 mm)
Recommended mounting hardware is:
SAE 4-40 (3mm)

Parts Listing

1 3800-133 PCB
2 ULN2803A relay drivers

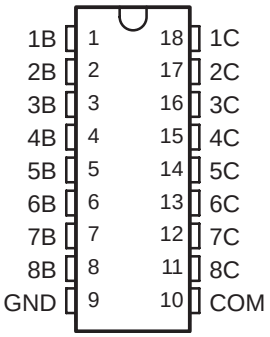
Glossary

References

Texas Instruments ULN2803A datasheet (attached).

- **500-mA Rated Collector Current (Single Output)**
- **High-Voltage Outputs . . . 50 V**
- **Output Clamp Diodes**
- **Inputs Compatible With Various Types of Logic**
- **Relay Driver Applications**
- **Compatible with ULN2800A Series**

DW OR N PACKAGE
(TOP VIEW)



description/ordering information

The ULN2803A is a high-voltage, high-current Darlington transistor array. The device consists of eight npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be connected in parallel for higher current capability.

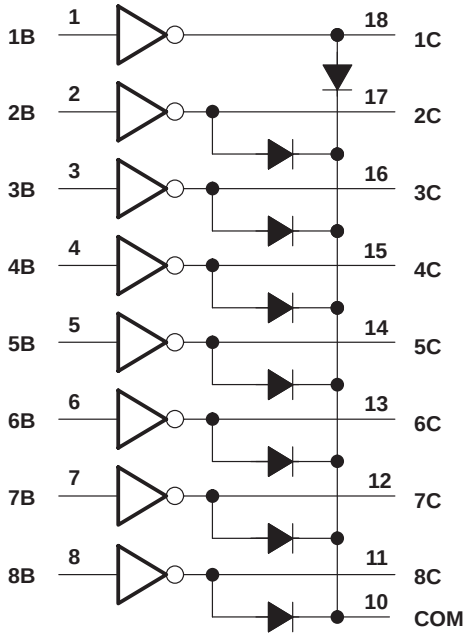
Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. The ULN2803A has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

ORDERING INFORMATION

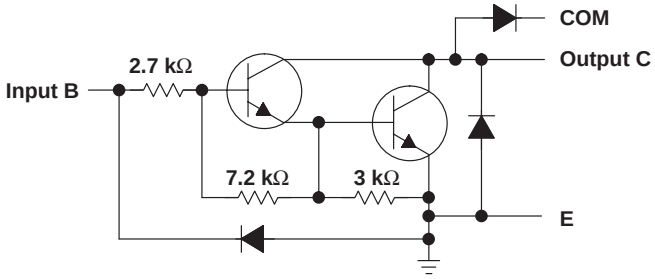
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP (N)	Tube of 20	ULN2803AN	ULN2803AN
	SOIC (DW)	Tube of 40	ULN2803ADW	ULN2803A
		Reel of 2000	ULN2803ADWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

logic diagram



schematic (each Darlington pair)



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Collector-emitter voltage . . . . . 50 V
Input voltage (see Note 1) . . . . . 30 V
Continuous collector current . . . . . 500 mA
Output clamp diode current . . . . . 500 mA
Total substrate-terminal current . . . . . −2.5 A
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DW package . . . . . 73.14°C/W
N package . . . . . 62.66°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the emitter/substrate terminal GND.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CEX}	Collector cutoff current	V_{CE} = 50 V, See Figure 1	I_I = 0,			50	µA
$I_{I(off)}$	Off-state input current	V_{CE} = 50 V, T_A = 70°C,	I_C = 500 µA, See Figure 2	50	65		µA
$I_{I(on)}$	Input current	V_I = 3.85 V,	See Figure 3		0.93	1.35	mA
$V_{I(on)}$	On-state input voltage	V_{CE} = 2 V, See Figure 4	I_C = 200 mA			2.4	V
			I_C = 250 mA			2.7	
			I_C = 300 mA			3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_I = 250 µA, See Figure 5	I_C = 100 mA,		0.9	1.1	V
		I_I = 350 µA, See Figure 5	I_C = 200 mA,		1	1.3	
		I_I = 500 µA, See Figure 5	I_C = 350 mA,		1.3	1.6	
I_R	Clamp diode reverse current	V_R = 50 V,	See Figure 6			50	µA
V_F	Clamp diode forward voltage	I_F = 350 mA,	See Figure 7		1.7	2	V
C_i	Input capacitance	V_I = 0 V,	f = 1 MHz		15	25	pF

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_S = 50 V, C_L = 15 pF,	R_L = 163 Ω, See Figure 8		130		ns
t_{PHL}	Propagation delay time, high- to low-level output				20		
V_{OH}	High-level output voltage after switching	V_S = 50 V, See Figure 9	$I_O \approx$ 300 mA,	V_S − 20			mV

PARAMETER MEASUREMENT INFORMATION

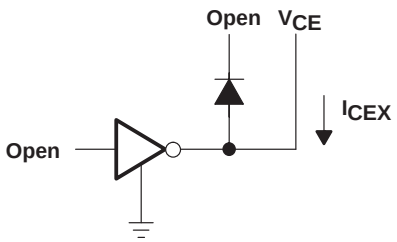


Figure 1. I_{CEX} Test Circuit

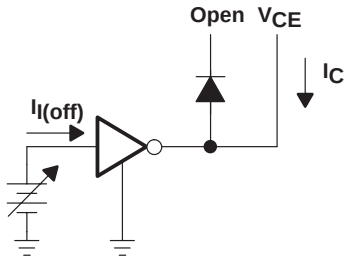


Figure 2. $I_{I(off)}$ Test Circuit

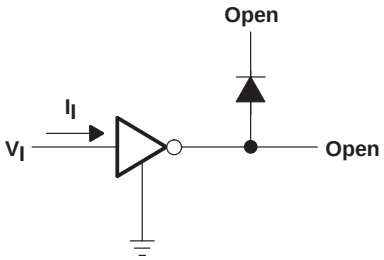


Figure 3. $I_{I(on)}$ Test Circuit

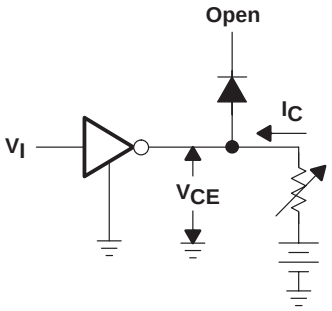


Figure 4. $V_{I(on)}$ Test Circuit

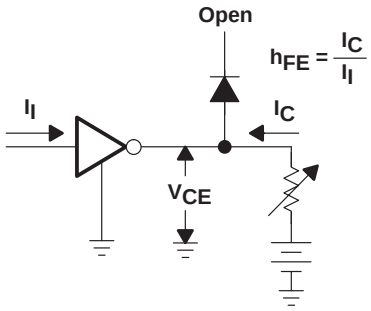


Figure 5. h_{FE}, $V_{CE(sat)}$ Test Circuit

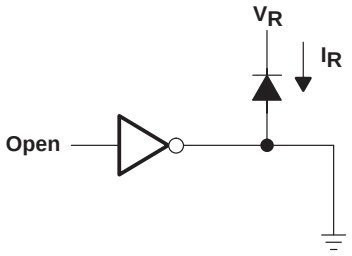


Figure 6. I_R Test Circuit

PARAMETER MEASUREMENT INFORMATION

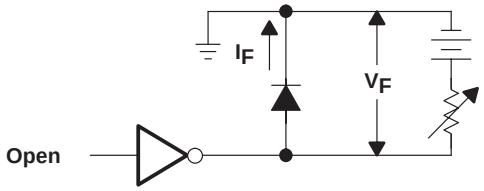
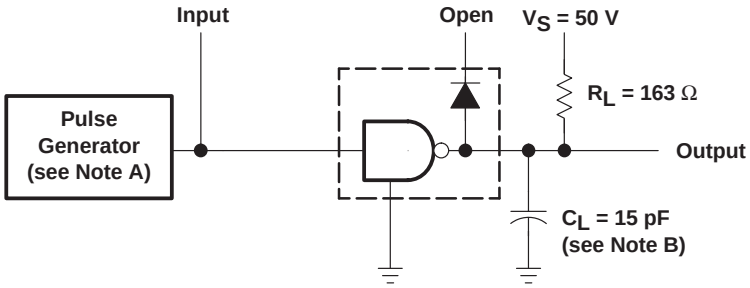
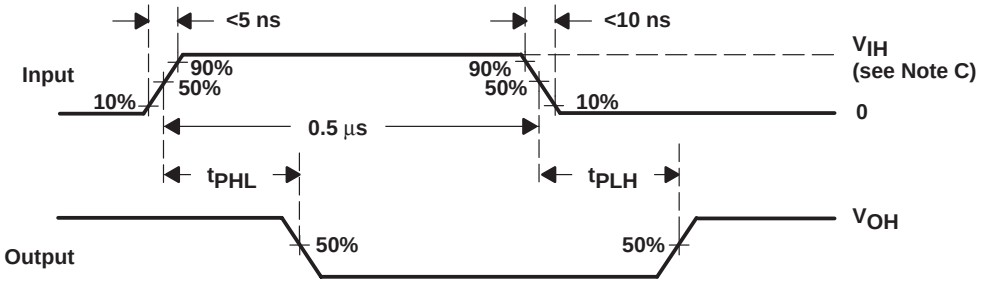


Figure 7. V_F Test Circuit



Test Circuit

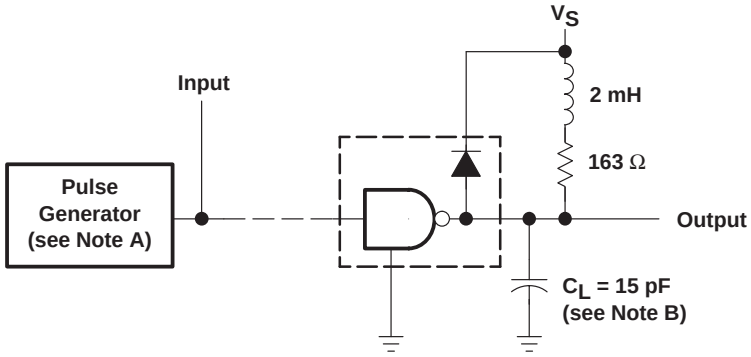


Voltage Waveforms

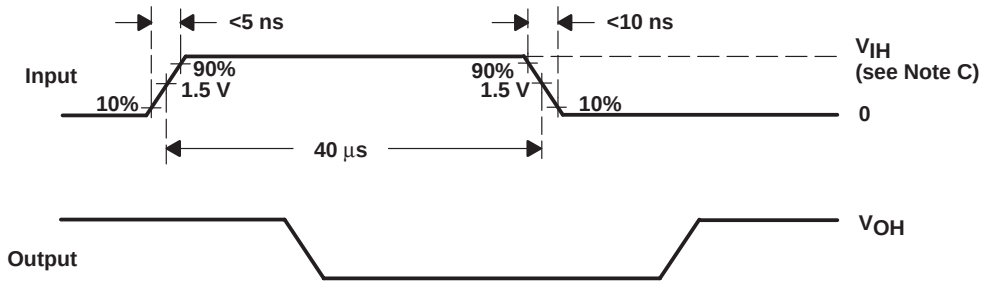
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. V_{IH} = 3 V

Figure 8. Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION



Test Circuit



Voltage Waveforms

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 KHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. V_{IH} = 3 V

Figure 9. Latch-Up Test